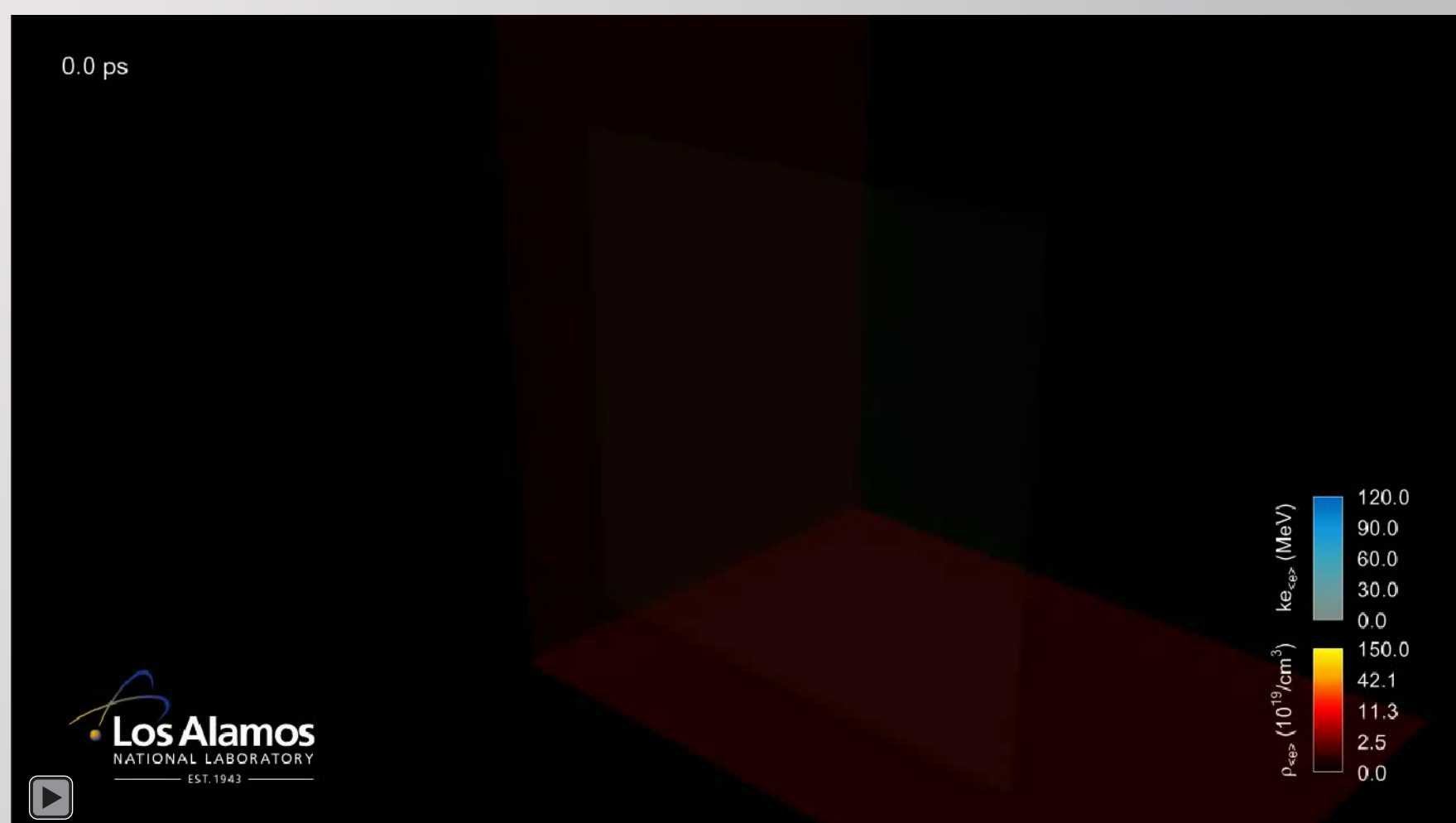


# Accelerated HPC Symposium 2012

May 14-17 SAN FRANCISCO BAY AREA

(Co-located with GPU Technology Conference)



## What are we about?

Much of the really exciting innovation in high-performance computing (HPC) is coming from accelerators, either in the form of GPGPUs or heterogeneous processors. Although there is growing vendor recognition of some of the issues that are specific to supercomputing, an ongoing consideration for the HPC community is that *the economies of scale that drive commodity technology development do not always share the concerns of power, scalability, and fault tolerance that are vital to the success of large-scale scientific computing efforts.* This symposium will seek to identify these issues and discuss strategies for dealing with them. The resulting dialogue will be summarized to provide vendors with new information on how their technologies are being used and on what changes or additions might aid in greater adoption.

## What are our goals?

- Continue the discussion of how accelerator technologies can be leveraged in innovative ways to advance the state-of-the-art for simulations on large-scale systems
- Explore hardware and software requirements for designing systems that can meet the requirements of power, scalability, and fault tolerance needed to reach the next level in HPC
- Understand how legacy codes can be adapted to make use of modern computing architectures
- Provide constructive feedback to the vendor community to aid in the adoption of accelerated technologies

## Workshop submissions are now open!

Scan the QR symbol or visit  
[www.lanl.gov/conferences/AHCPS](http://www.lanl.gov/conferences/AHCPS)

*Deadline February 10, 2011*  
*Notification March 18, 2011*



Symposium Chair Ben Bergen, [bergen@lanl.gov](mailto:bergen@lanl.gov), 505-465-9316